

MOS Timing Mode Spectral Features and Possible Improvements

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Calibration Ops Meeting Vilspa
23-24 Mar 2004



Overview of current concerns

- Timing mode has poor DNL because:
 - Timing mode sequences free run
 - Design decision was therefore not to use Gatti because communication with the EMCR control processor would interrupt the timing flow
- Next slide explains Gatti and DNL

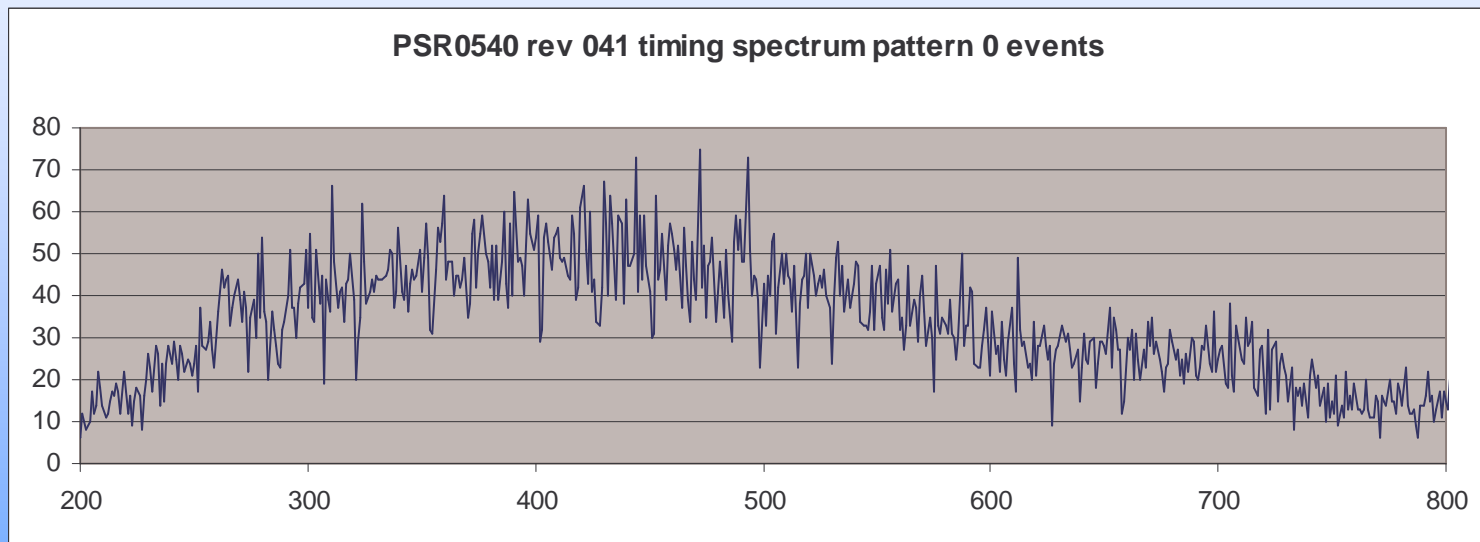
DNL and Gatti

DNL – Differential Noise Linearity is caused by different digital values of the ADC having differing channel widths due to internal accuracy and noise.

Gatti – sliding scale baseline offset technique which applies a precise analogue offset before ADC conversion and removes it digitally from the result. In the case of the MOS, this offset is changed every frame in imaging modes.

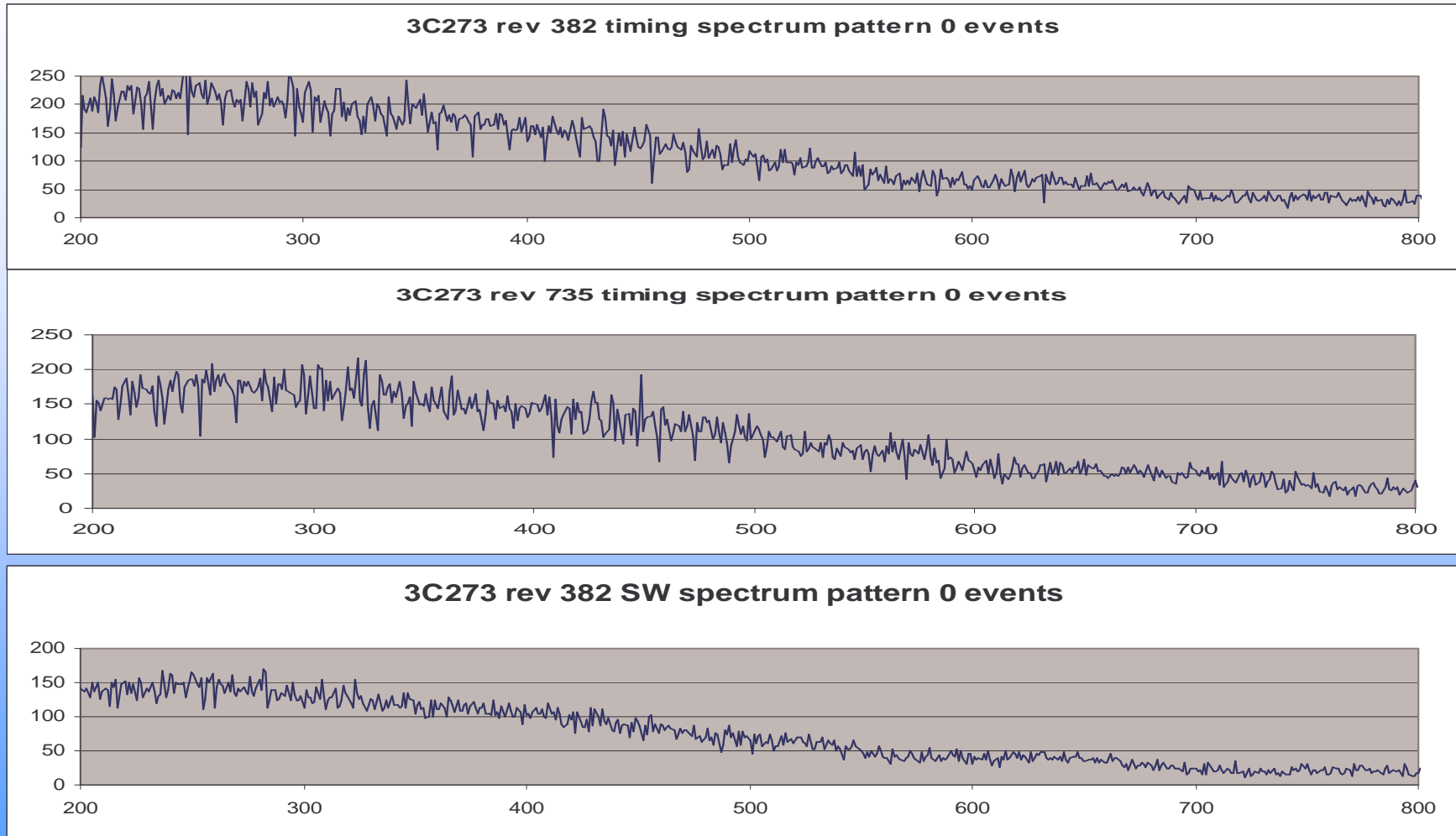
Gatti causes the DNL to be smeared out over the width of the offset range (256 DN for MOS), and become invisible.

PSR0540 spectrum

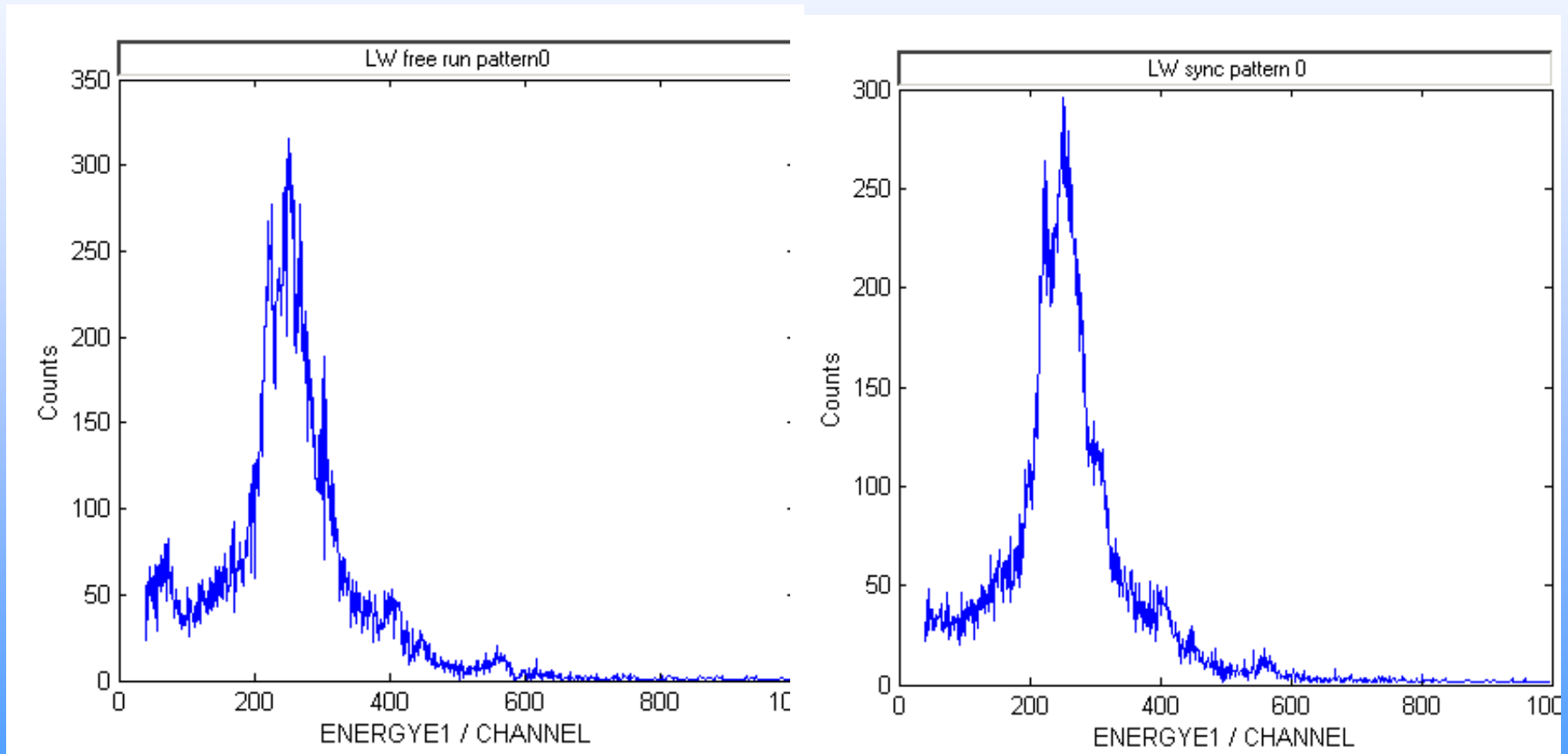


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3C273 spectra with/without DNL

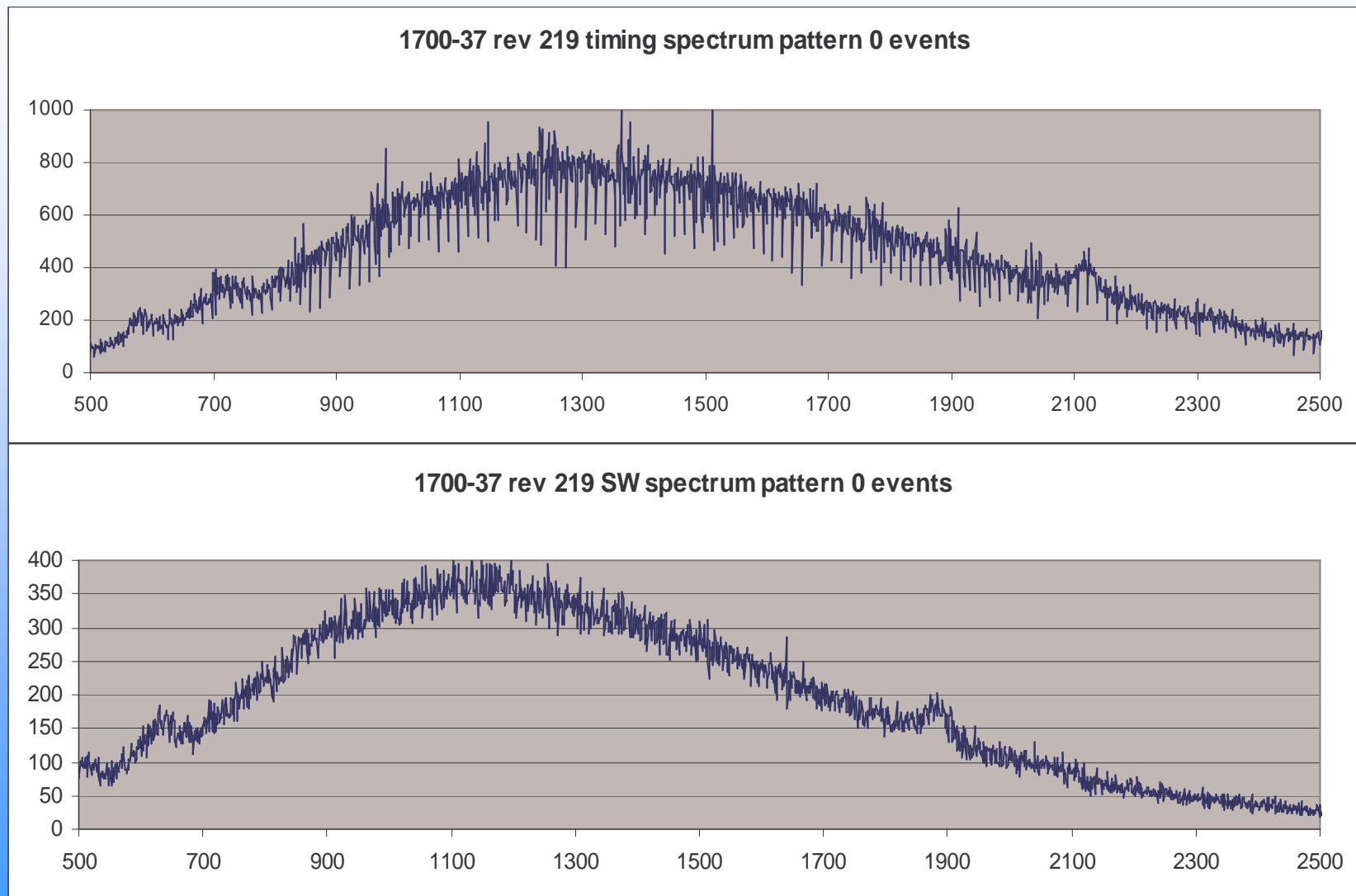


Capella LW rev 0043 without/with Gatti



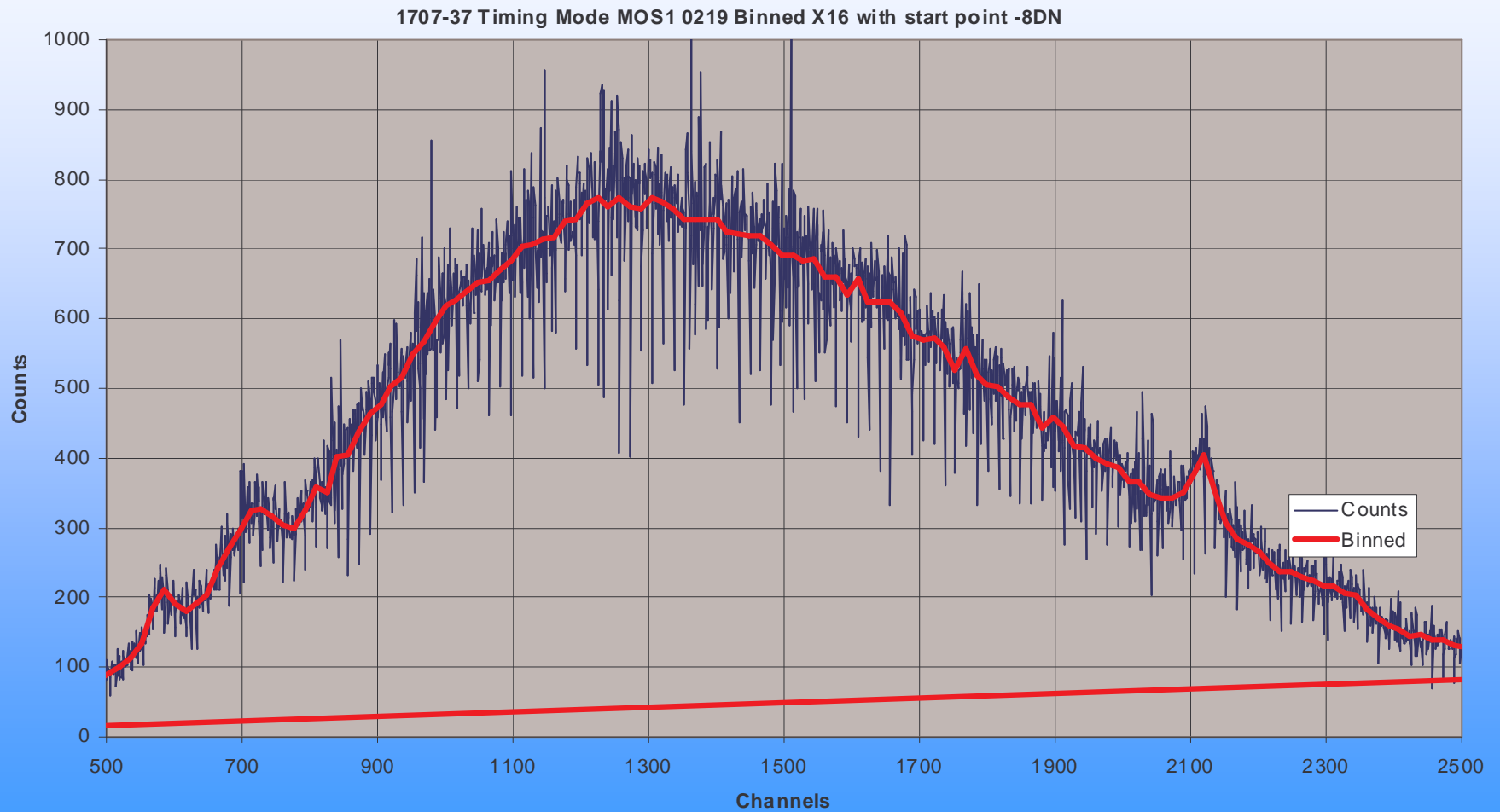
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1700-37 rev 219 comparison



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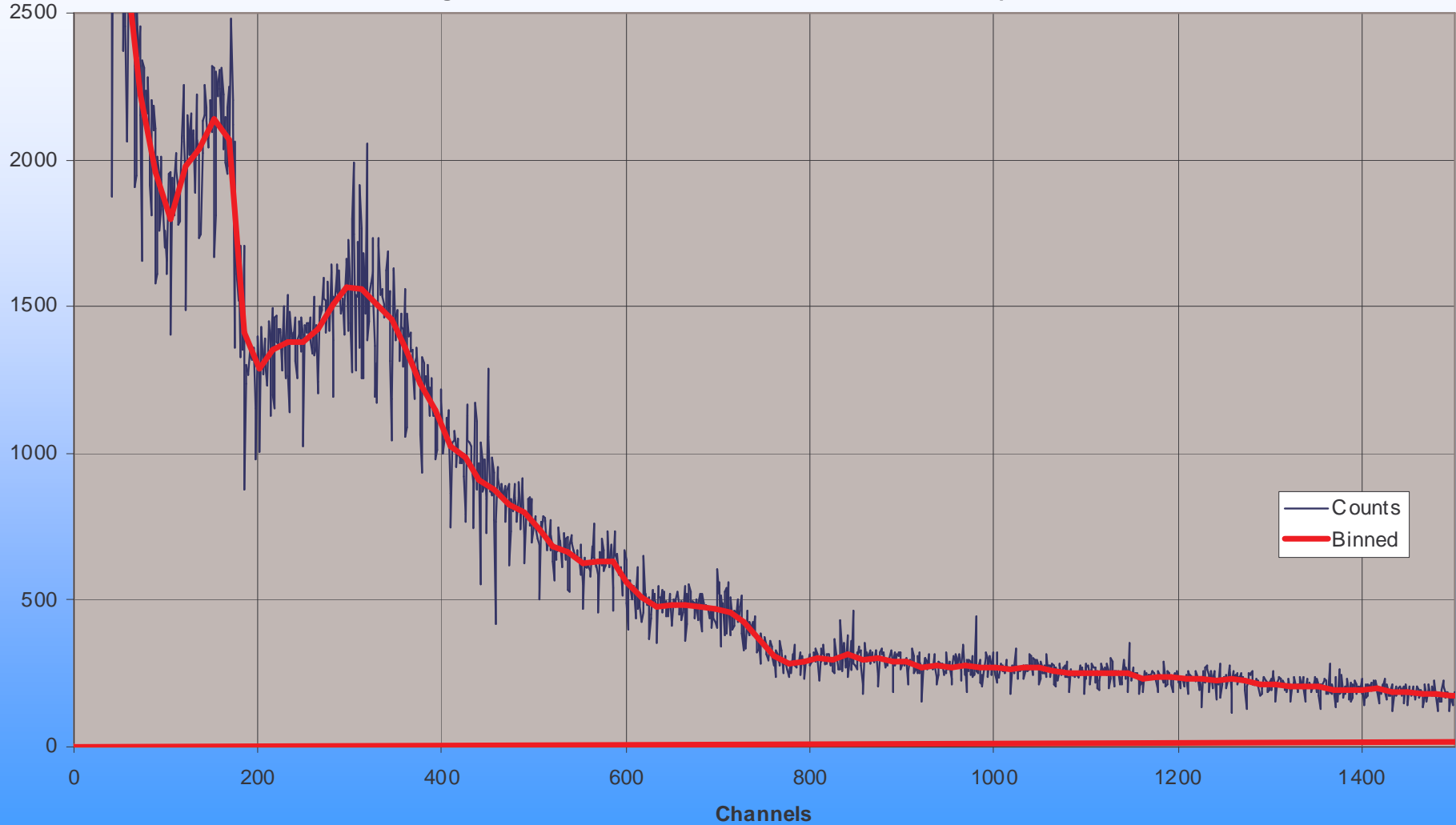
Binning



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Binning2

Her X1 Timing Mode MOS1 0207_0134120101 Binned X16 with start point -8DN



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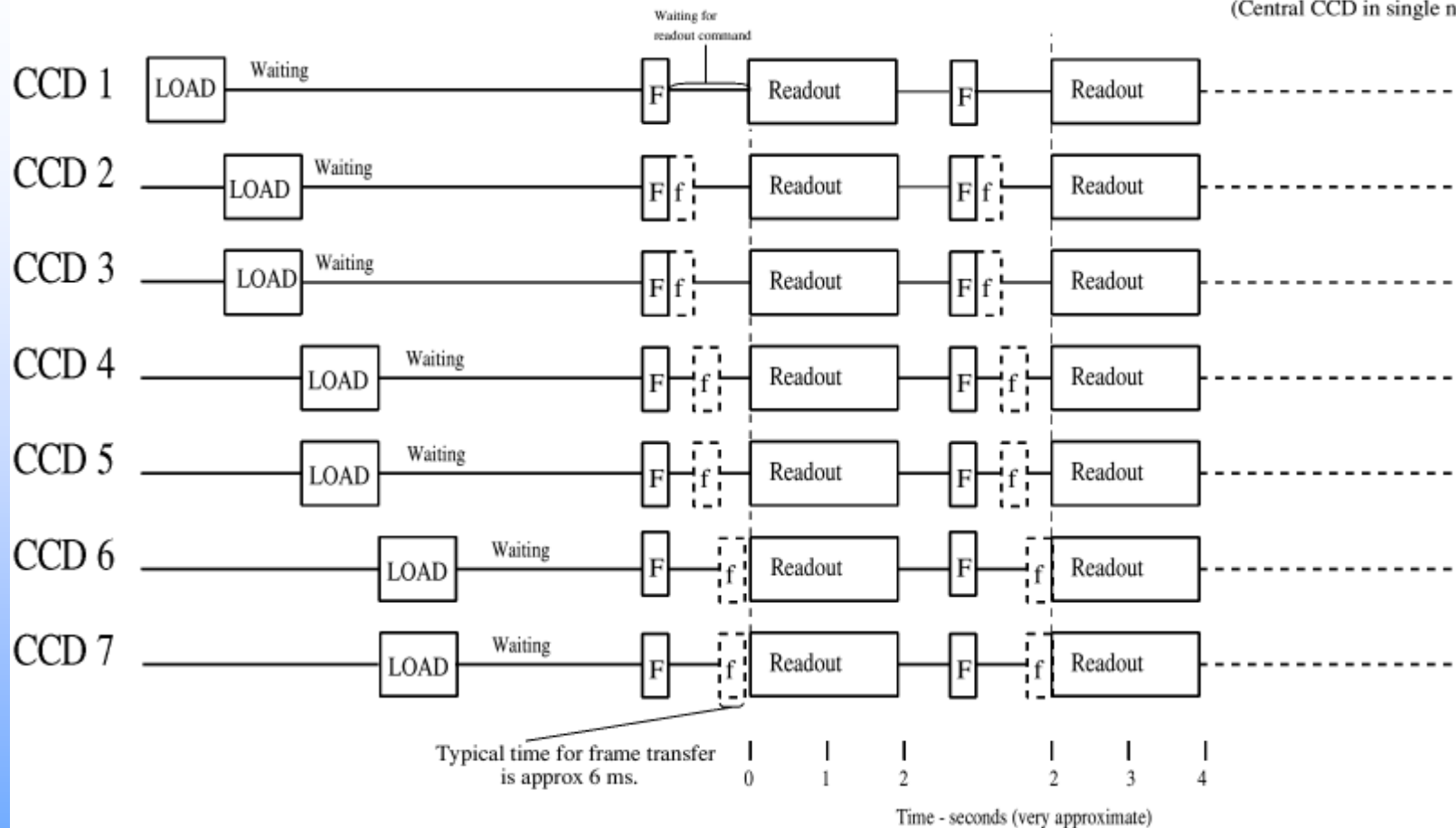
Alternative – bring back Gatti

- Gatti DAC could be incremented by EMCR every timing frame
- Slight asynchronism in setting and subtracting could result in a few events getting 1DN error (negligible effect compared with energy resolution)
- Discuss with Saclay if software mod is needed

Timing Diagram for Readout of Central CCD and 6 Peripheral CCDs on XMM EPIC MOS Camera

Revised 4 April 1995

(Central CCD in single node readout mode)



Notes:

F means: Controller sends FRAME TRANSFER CCD "N"

Readout means:
EMCR first sets MUX channel setting (if not already set)
Then the Gatti values for the one or two associated ADC channels
On receiving readout command bit the relevant sequencer outputs the CCD store section(s) to the EDU(s) and sends EOF with last pixel.

↳ Sequencer "S" waits for delay D(S) in order to stagger frame transfers
 - - Sequencer "S" sends EOI to EDU
 - f Sequencer "S" transfers IMAGE>STORE of CCD "N" and "N+1"
 - - then waits for readout command from EMCR

* Note Sequencer 1 is used for CCD1 only, but sequencer 2 is for CCDs 2 & 3, seq 3 for 4 & 5, and seq 4 for 6 & 7

Timing mode sequence in the EMCR/EDU

